

IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) A device comprising:

- a first major exterior surface;
- a second major exterior surface, at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads;
- a signal carrying plated through hole terminating at the at least one of the first major surface and the second major exterior surface;
- a pad between the first major surface and the second major surface, the signal carrying plated through hole connected to the pad;
- an antipad element substantially surrounding the pad;
- a plane metallization layer within the device substantially surrounding the pad and the antipad;
- a plated through hole attached to the plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including the plurality of component mounting pads, the plated through hole attached to the plane metallization layer, and electrically isolated from the plurality of component mounting pads; and
- a circuit tester for determining if a current will flow between the pad and the signal carrying via, and the plane metallization layer to test the spacing of a plane metallization layer from a signal through hole that passes through the plane metallization layer.

2. (Original) The device of claim 1 wherein the plane metallization layer is a power plane.

3. (Original) The device of claim 1 wherein the plane metallization layer is a ground plane.

4. (Original) The device of claim 1 wherein the plane metallization layer is a reference voltage plane.

5. (Previously Presented) The device of claim 1 further comprising a signal carrying plated through hole which passes through the plane metallization layer within the device and terminates at the component mounting pad at the at least one of the first major exterior surface and the second major exterior surface including the plurality of component mounting pads.
6. (Previously Presented) The device of claim 5 wherein the signal carrying plated through hole which passes through the plane metallization layer is electrically isolated from the plane metallization layer and is connected to the component mounting pad at the at least one of the first major exterior surface and the second major exterior surface including the plurality of component mounting pads.
7. (Original) The device of claim 1 wherein the device forms a printed circuit board.
8. (Original) The device of claim 1 wherein the device forms a semiconductor chip.
9. (Original) The device of claim 1 wherein the plated through hole is a via.
10. (Previously Presented) A system comprising:
- a processor;
 - a memory communicatively coupled to the processor; and
 - a device associated with at least one of the memory or the processor further including:
 - a first major exterior surface;
 - a second major exterior surface, at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads;
 - a signal carrying plated through hole terminating at the at least one of the first major surface and the second major exterior surface;
 - a pad between the first major surface and the second major surface, the signal carrying plated through hole connected to the pad;
 - an antipad element substantially surrounding the pad;

a plane metallization layer substantially surrounding the pad and antipad within the device; and

a plated through hole attached to the plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including the plurality of component mounting pads, the plated through hole attached to the plane metallization layer electrically isolated from the plurality of component mounting pads; and

a circuit test apparatus for testing the spacing between the plane metallization layer and the pad associated with the signal carrying through hole.

11. (Original) The system of claim 10 wherein the device is a printed circuit board.
12. (Original) The system of claim 10 wherein the device is a portion of a semiconductor chip.
13. (Original) The system of claim 10 wherein the plane metallization layer is a ground plane.
14. (Original) The system of claim 10 wherein the plane metallization layer is a power plane.
15. (Original) The system of claim 10 wherein the plane metallization layer is a reference voltage plane.
16. (Canceled)
17. (Original) A device comprising:
 - a first major exterior surface;
 - a second major exterior surface, at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads;
 - a first plane metallization layer within the device;
 - a second plane metallization layer within the device;
 - a first plane plated through hole attached to at least one of the first plane metallization layer and the second plane metallization layer and terminating at the at least one of the first

major exterior surface and the second major exterior surface including a plurality of component mounting pads, the first plated through hole attached to the plane metallization layer electrically isolated from the plurality of component mounting pads.

18. (Original) The device of claim 17 further comprising a signal carrying plated through hole which passes through the first plane metallization layer and is electrically isolated from the first plane metallization layer, the signal carrying plated through hole passes through the second plane metallization layer and is electrically isolated from the second plane metallization layer, the signal carrying through hole connected to a component mounting pad at the at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads.

19. (Original) The device of claim 18 wherein the first plane plated through hole is attached to both the first plane metallization layer and the second plane metallization layer.

20. (Original) The device of claim 18 wherein the first plane plated through hole is attached to the first plane metallization layer, the device further comprising a second plane plated through hole attached to the second plane metallization layer, the second plated through hole terminating at the at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads, the second plated through hole attached to the second plane metallization layer electrically isolated from the plurality of component mounting pads.

21.-27. (Canceled)

28. (Previously Presented) A device comprising:

- a first major exterior surface;
- a second major exterior surface, at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads;
- a feature positioned within the device;

a plated through hole attached to a plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads, the plated through hole attached to the plane metallization layer within the device, and electrically isolated from the plurality of component mounting pads, wherein the feature positioned within the device passes through the plane metallization layer and is isolated from the plane metallization layer; and

a test device electrically coupled to the feature for testing the spacing between the feature and the plane metallization layer.

29. (Previously Presented) The device of claim 28 wherein the feature is an electrical trace.

30. (Previously Presented) The device of claim 28 wherein the feature is a signal carrying through hole.

31. (Previously Presented) The device of claim 28 wherein the test device includes a pad on one of the first major surface or the second major surface.

32. (Previously Presented) The device of claim 28 wherein the test device is a probe from a circuit tester.

33. (Previously Presented) The device of claim 28 wherein the test device is a circuit tester.